

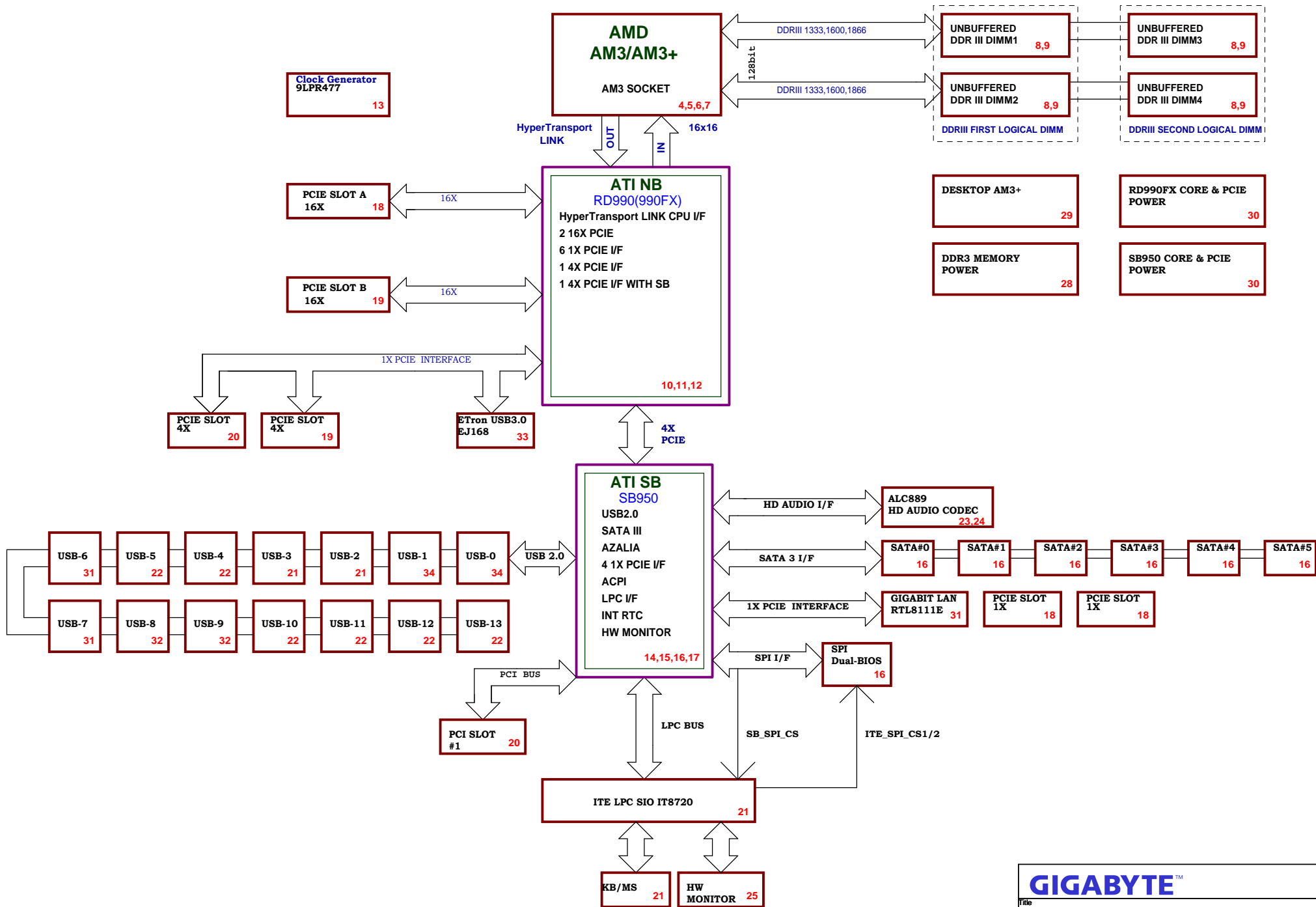
[illegible][illegible][illegible][illegible]

1

Circuit or PCB layout change for next version

P-Code:
U98145-0

[illegible][illegible]1



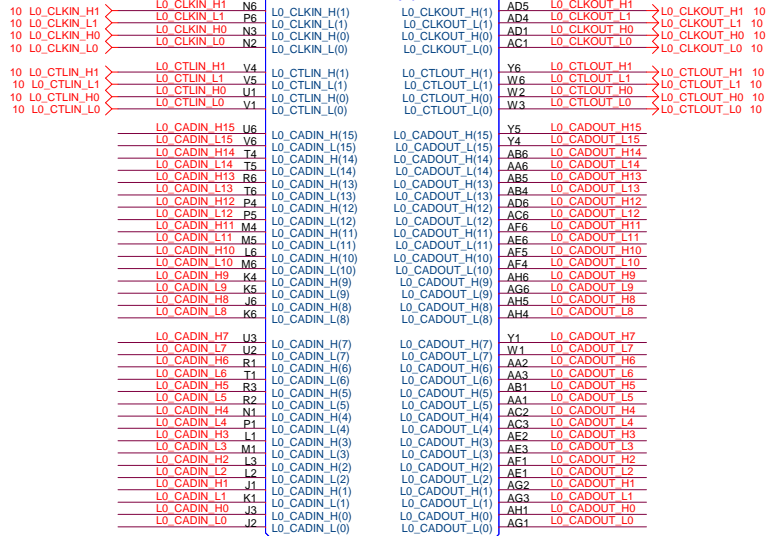
L0_CADIN_L[0..15] <L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 10

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

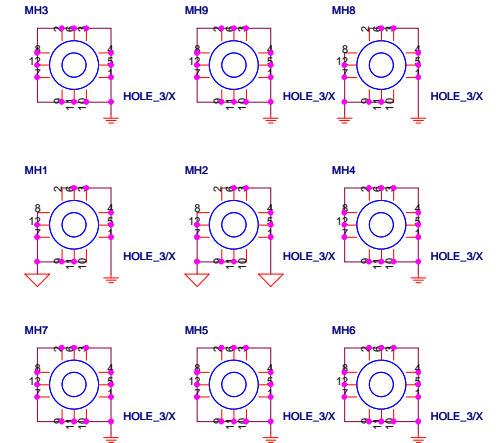
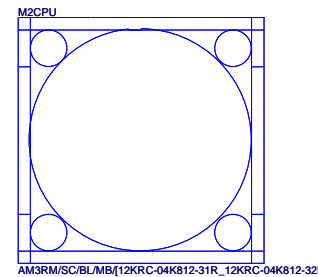
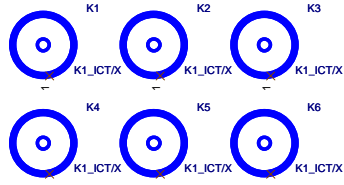
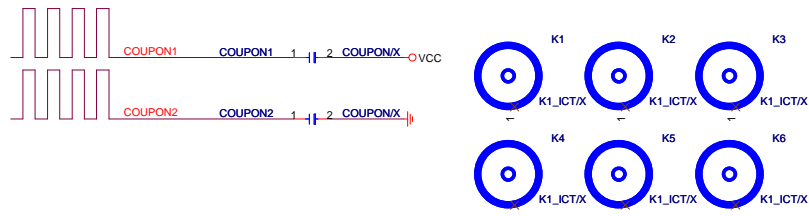
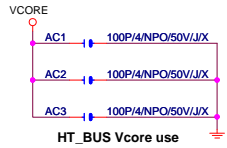
VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

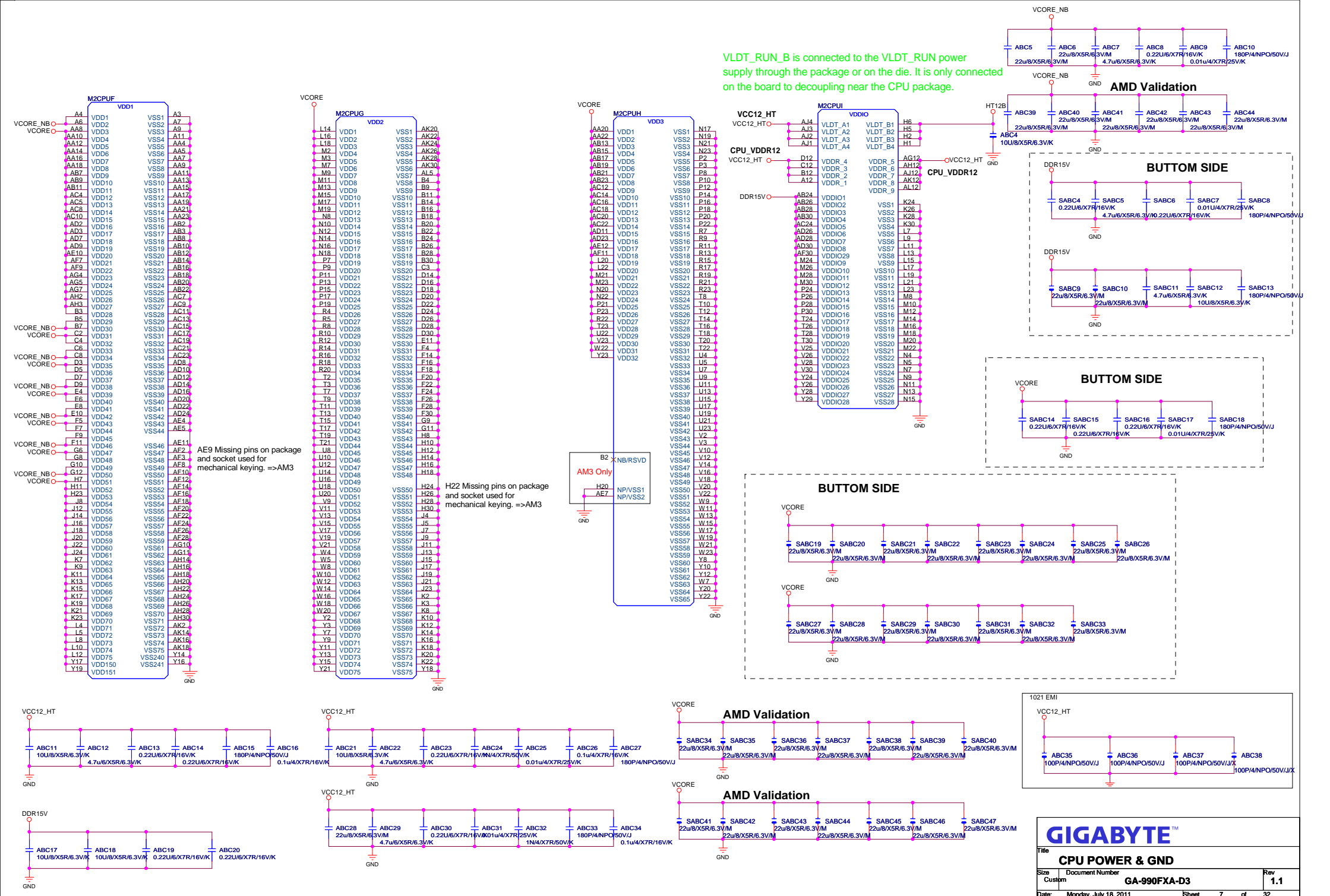


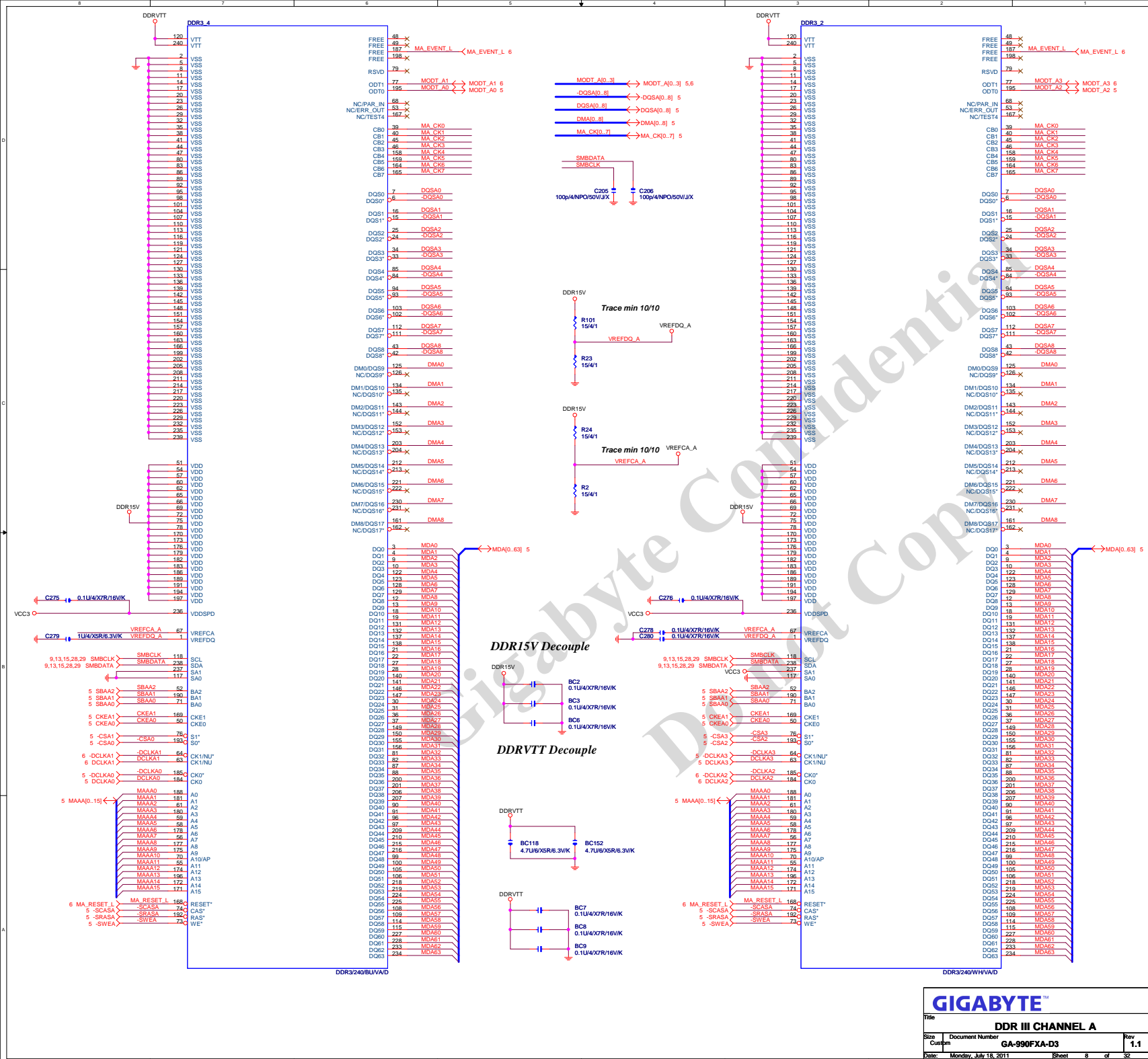
CPU-SK941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

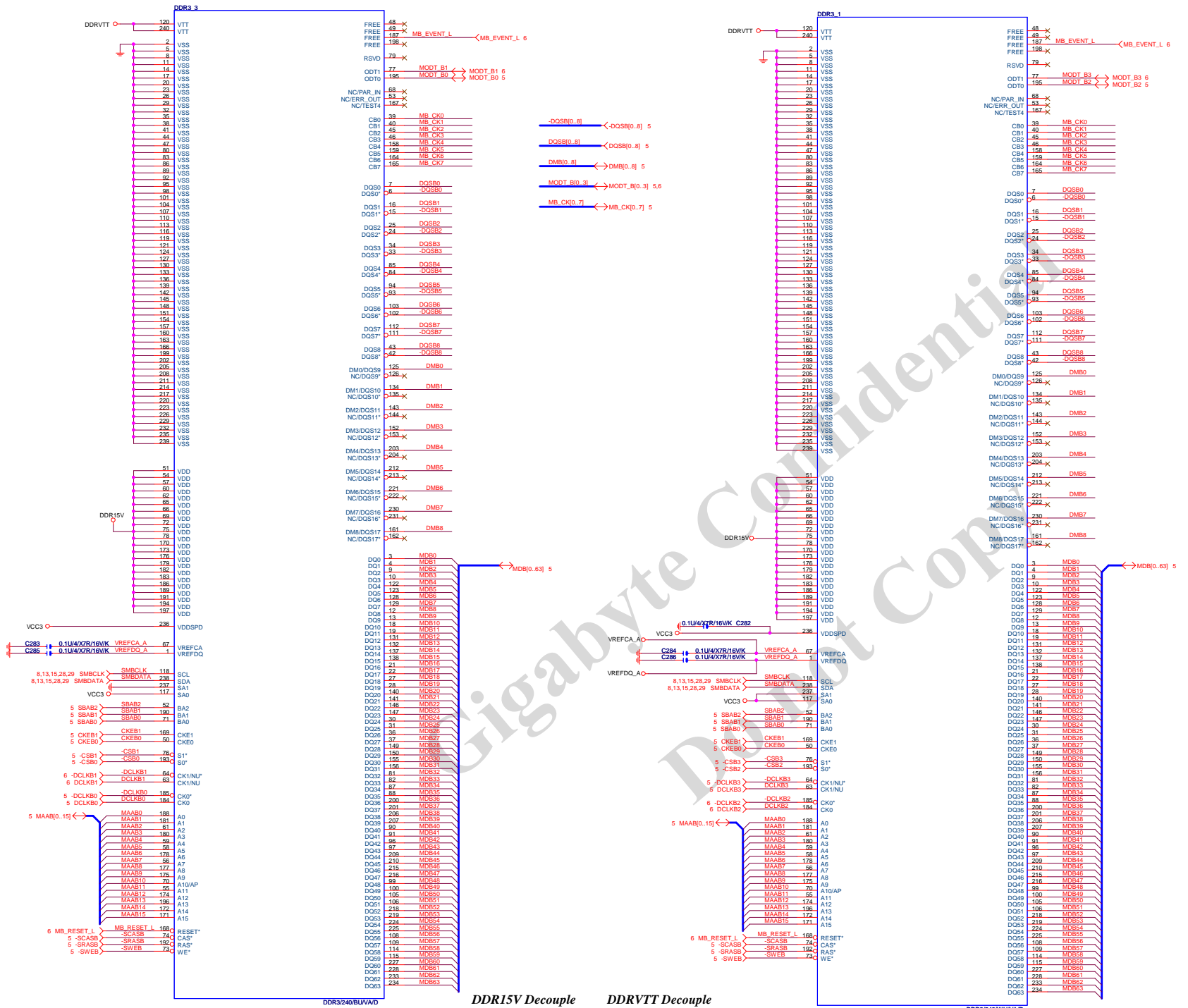


GIGABYTE		
Title COVER SHEET		
Size Custom	Document Number GA-990FXA-D3	Rev 1.1
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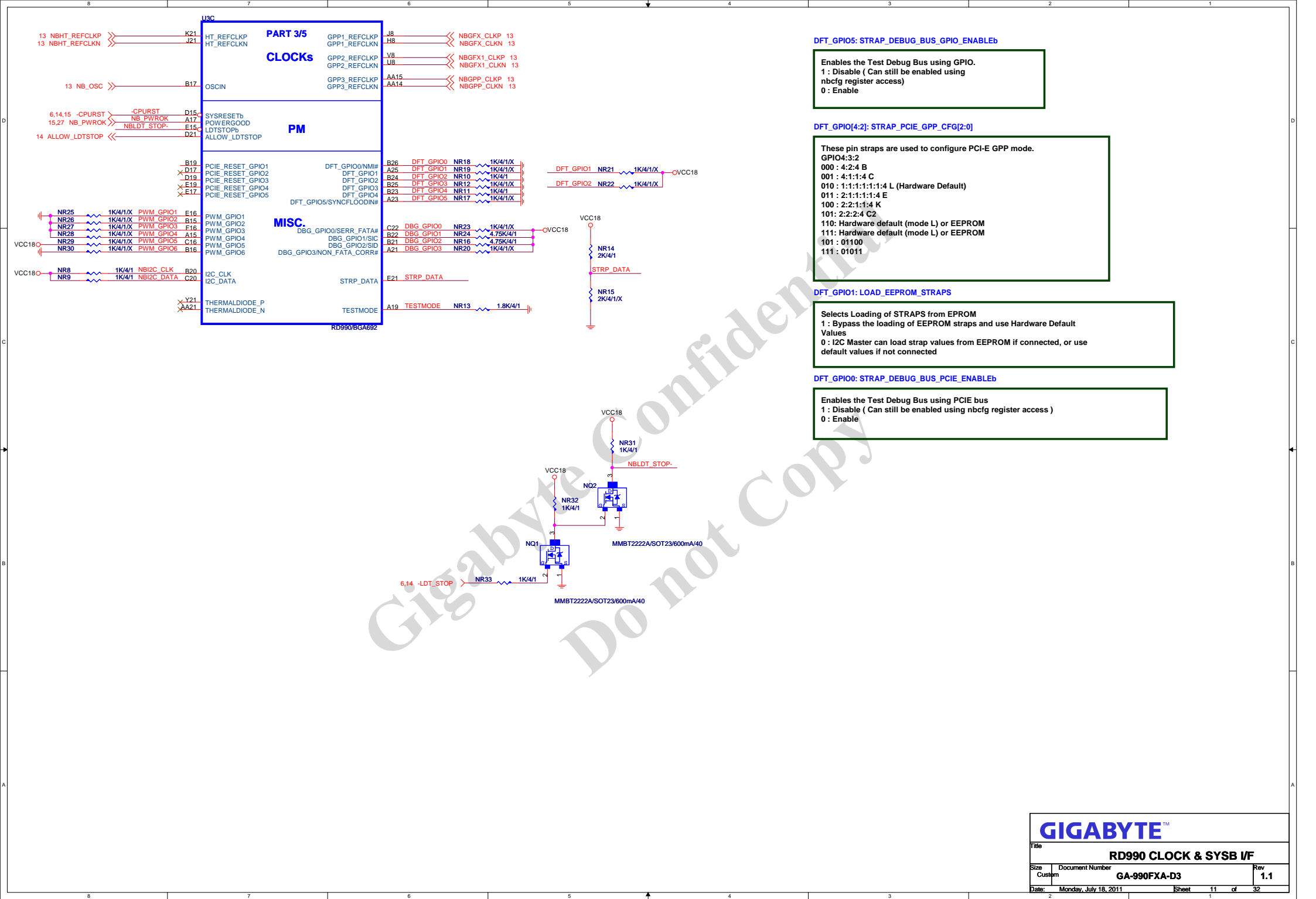
VLDI_RUN_B is connected to the VLDI_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

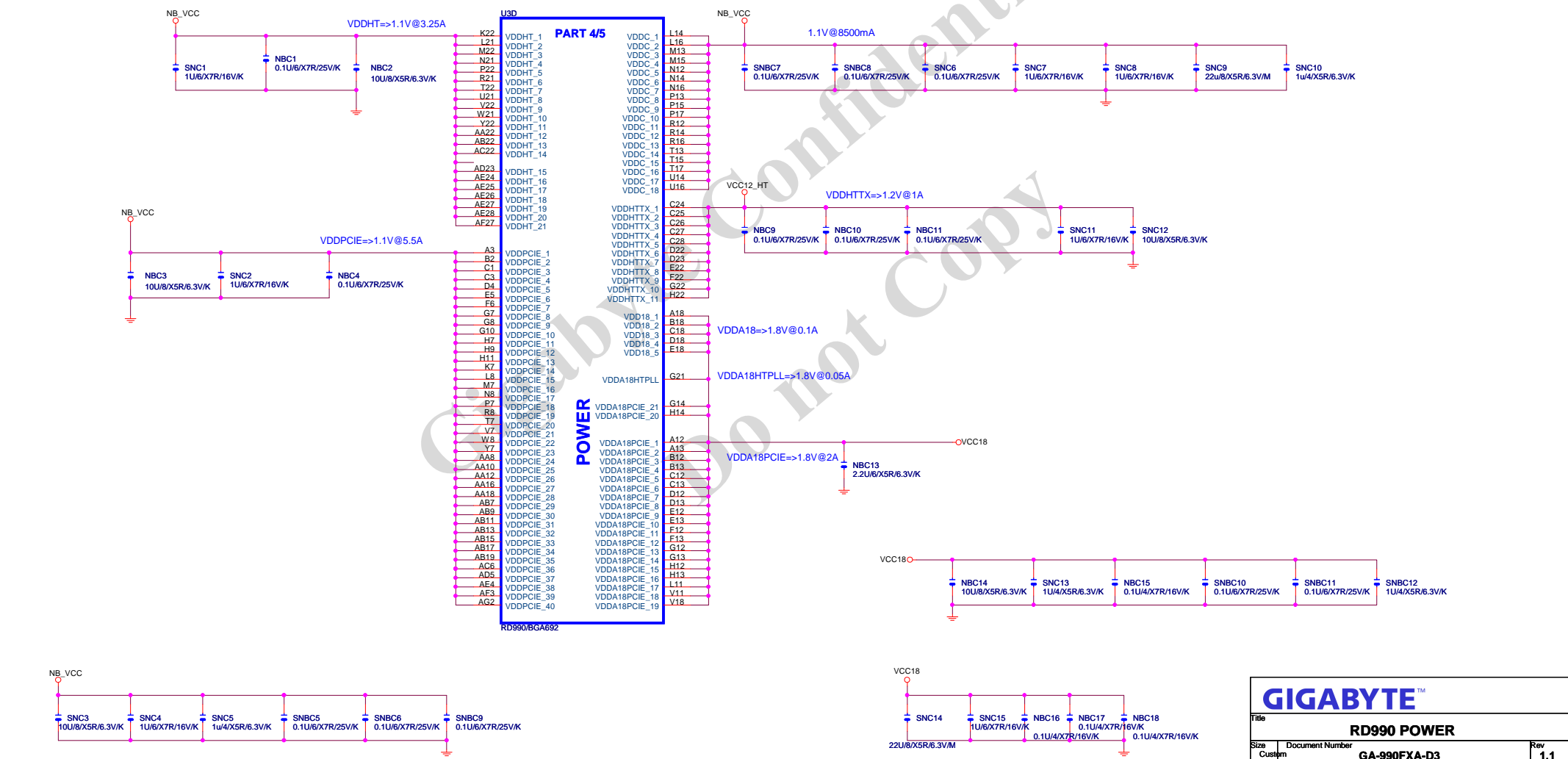
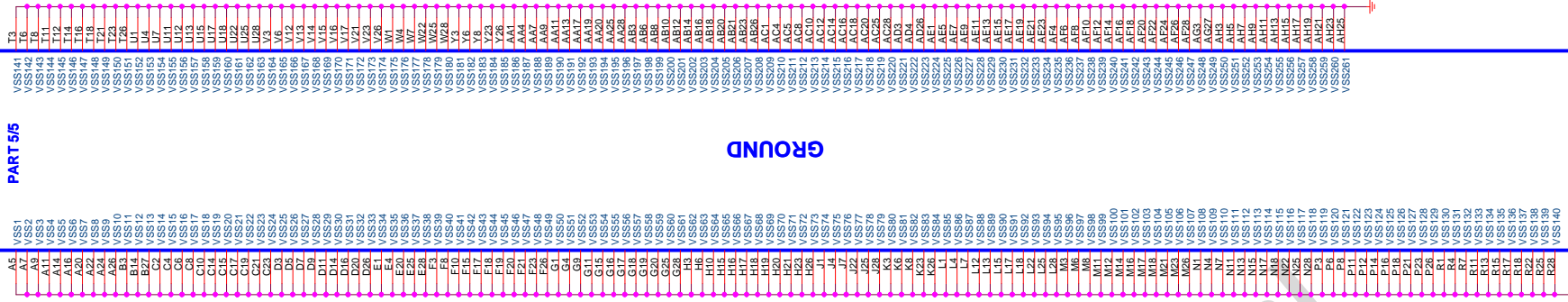


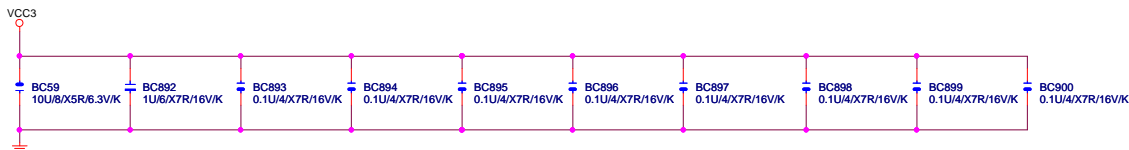




DDR15V Decouple DDRVTT Decouple



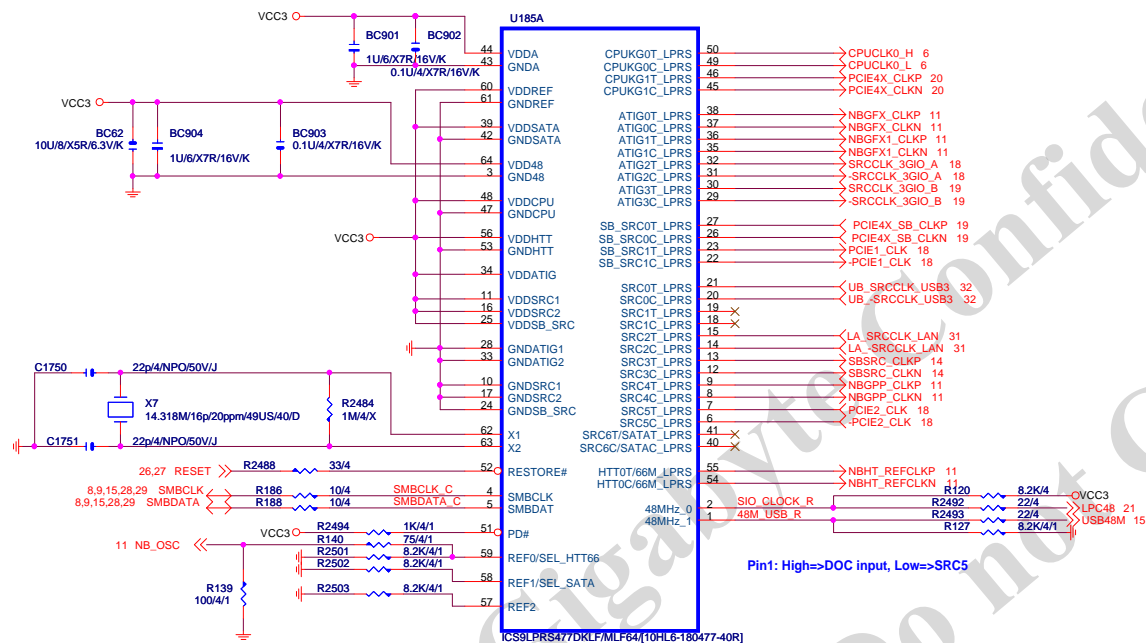




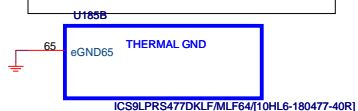
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE

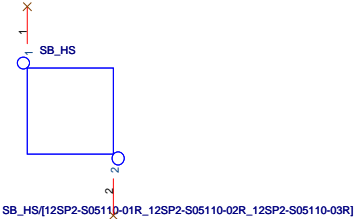
Title: **ICS9LPRS477**

Size: Custom Document Number: **GA-990FXA-D3** Rev: **1.1**

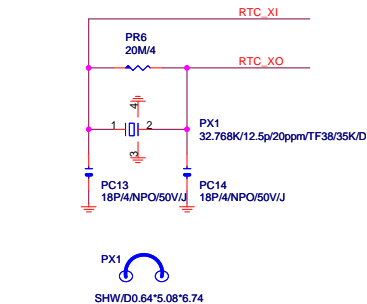
Date: Monday, July 18, 2011 Sheet: 13 of 32

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

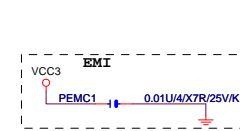
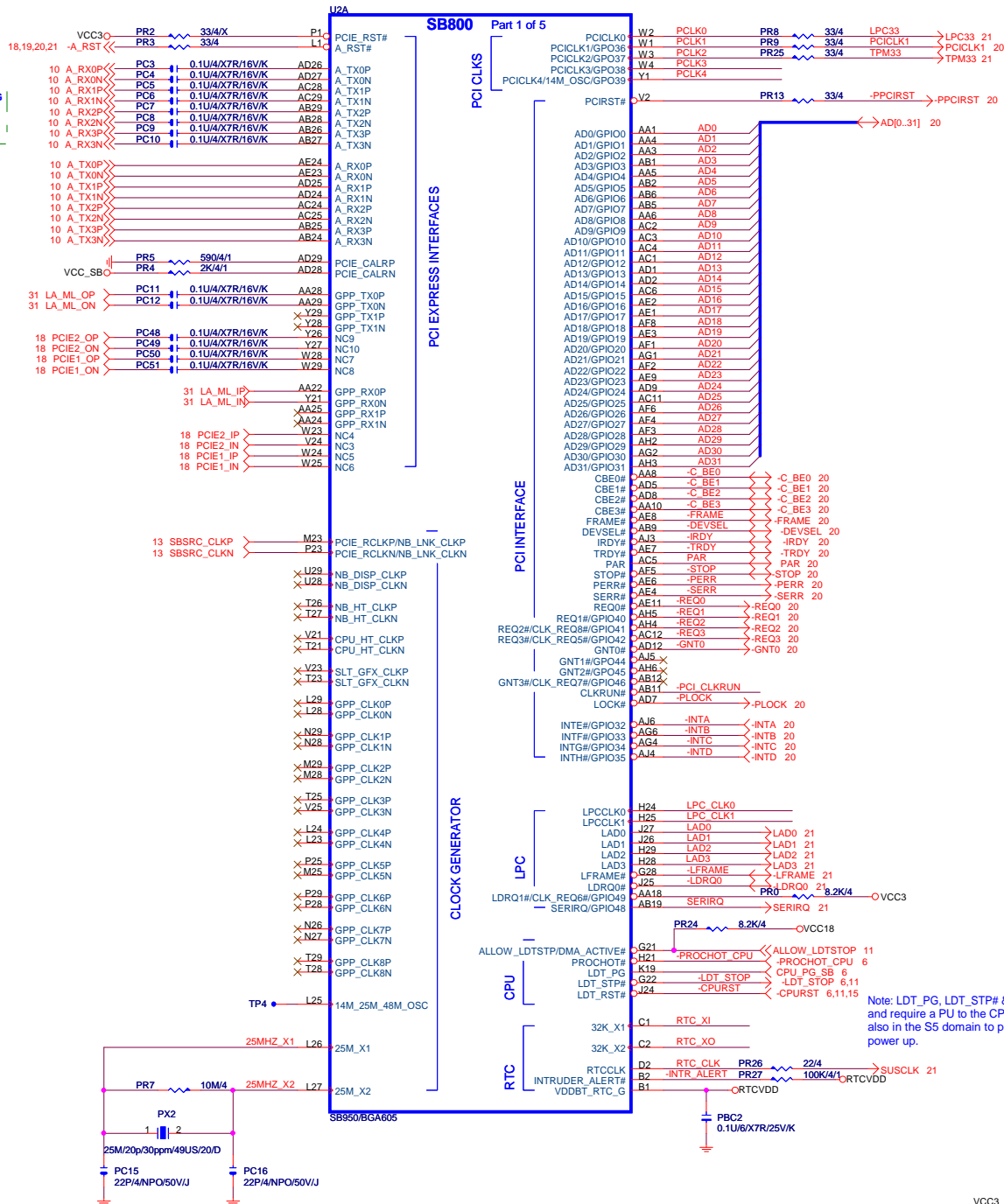
S.B HEATSINK



SB_HS[12SP2-S05110-01R_12SP2-S05110-02R_12SP2-S05110-03R]



SHW/D0.64*5.08*6.74



Low: Force PCIE GEN1, Up: Allow PCIE GEN2



PULL HIGH PULL LOW PULL HIGH PULL LOW

PCLK2 WATCHDOG TIMER ON NB_PWRGD ENABLED

PCLK3 USE DEBUG STRAPS

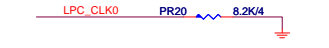
WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT

IGNORE DEBUG STRAPS

DEFAULT



BIOS after boot setting EC AOD-ACC



LPC_CLK0 Rev.A12

LPC_CLK1

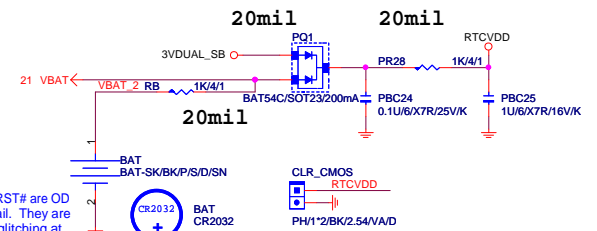
PULL HIGH PULL LOW PULL HIGH PULL LOW

IMC ENABLED AOD Extreme DISABLED

CLKGEN ENABLED

CLKGEN DISABLED

DEFAULT



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

GIGABYTE

ATI SB950 PCIE/PCI/CPU/LPC

Size Custom Document Number GA-990FXA-D3 Rev 1.1

Date: Monday, July 18, 2011 Sheet 14 of 32



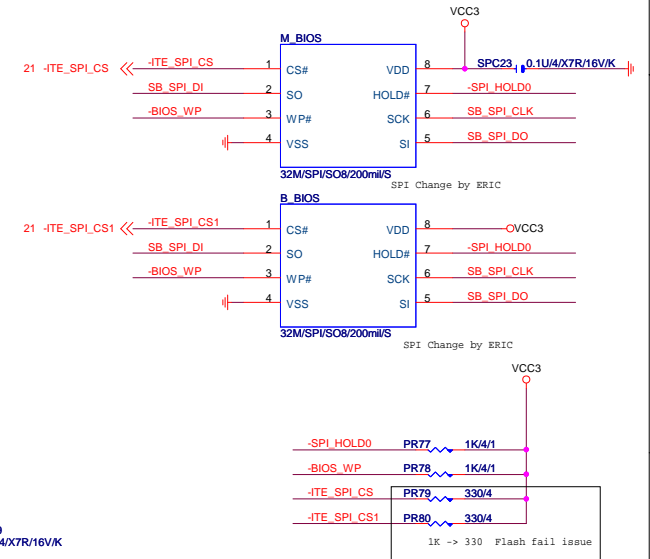
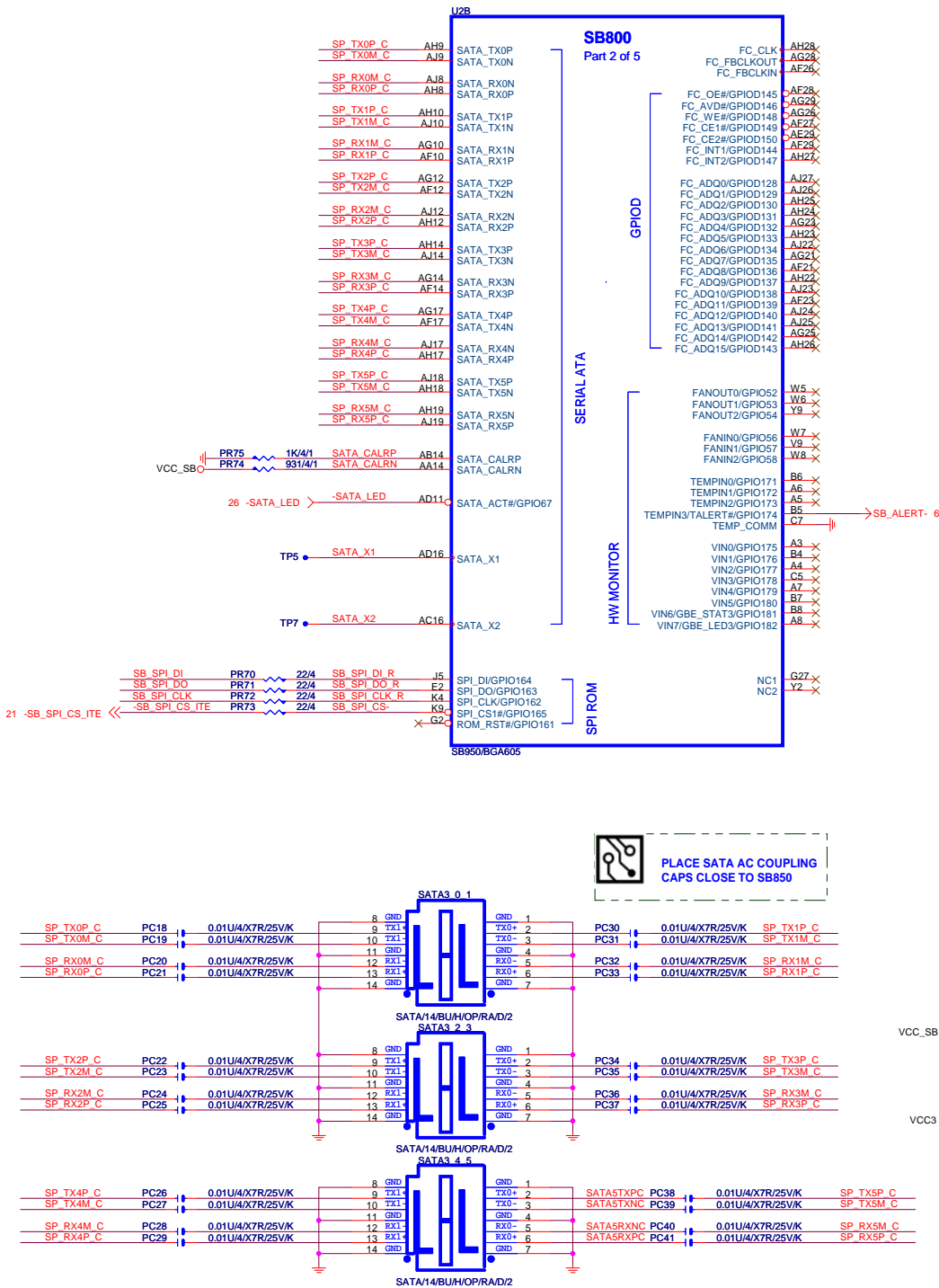
PLACE SATA CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK



PLACE SATA AC COUPLING
CAPS CLOSE TO SB850

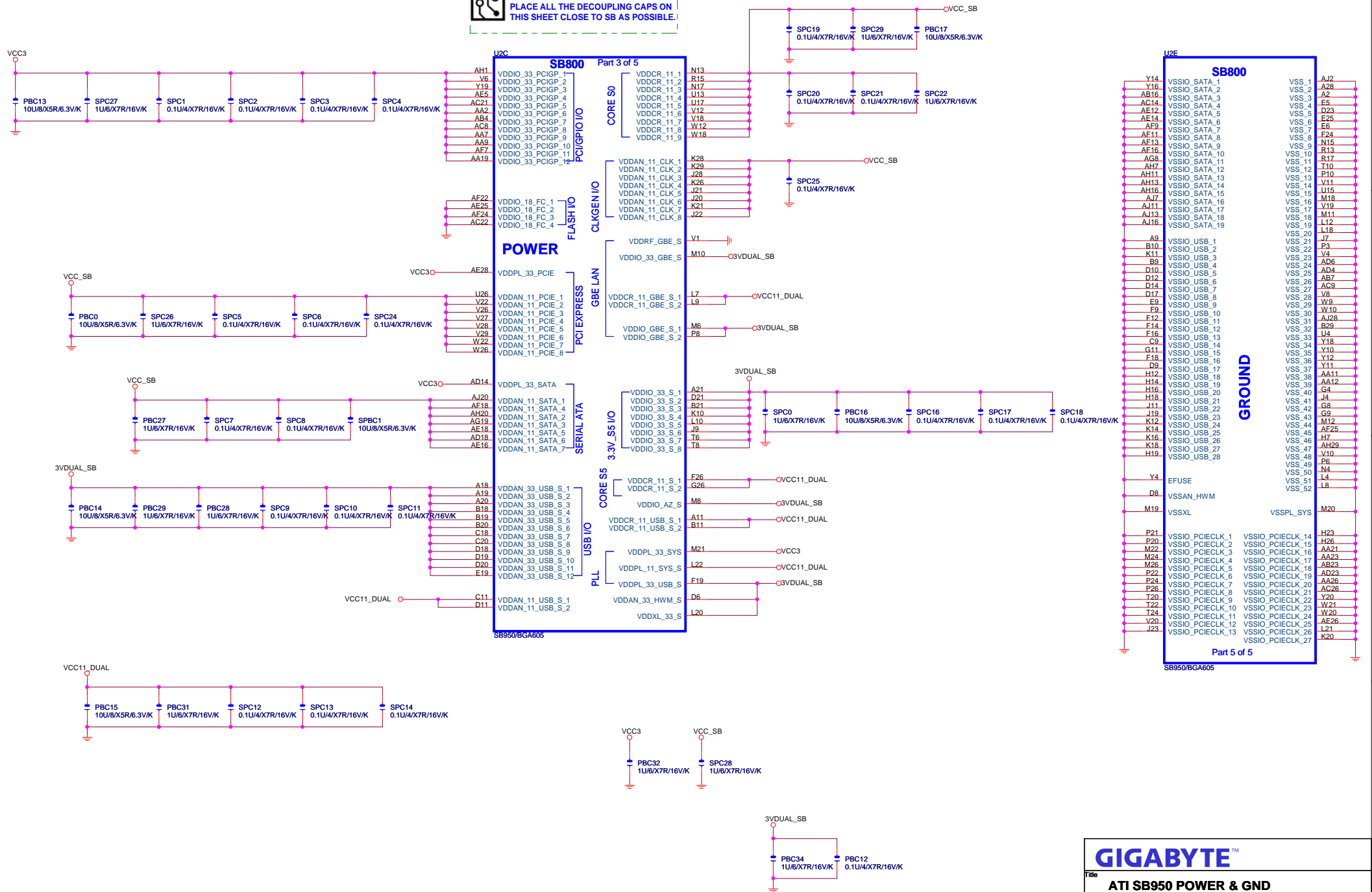


GIGABYTE™

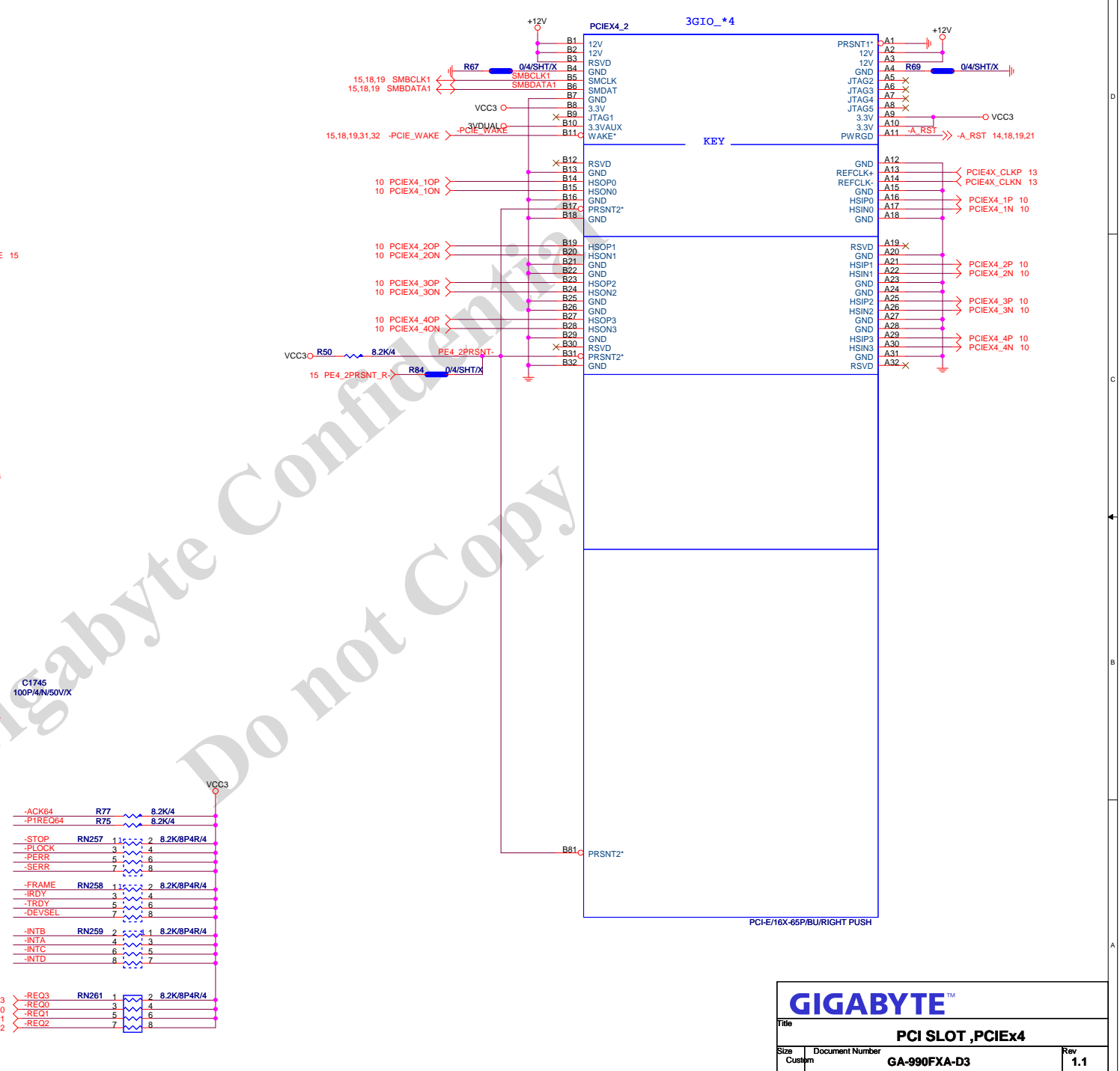
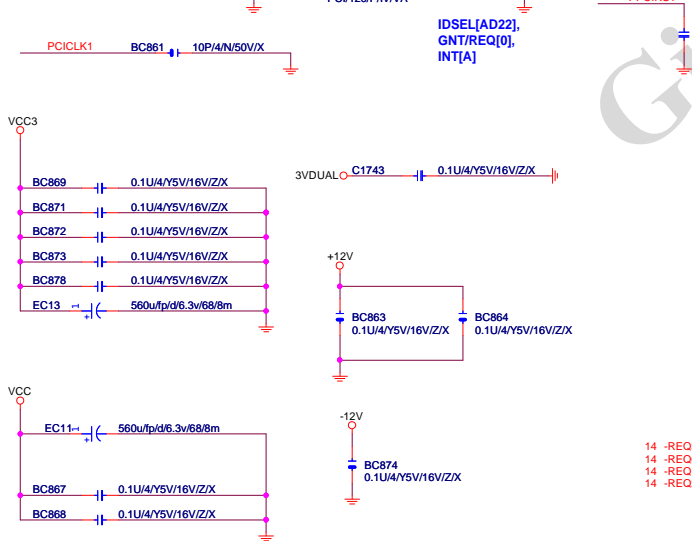
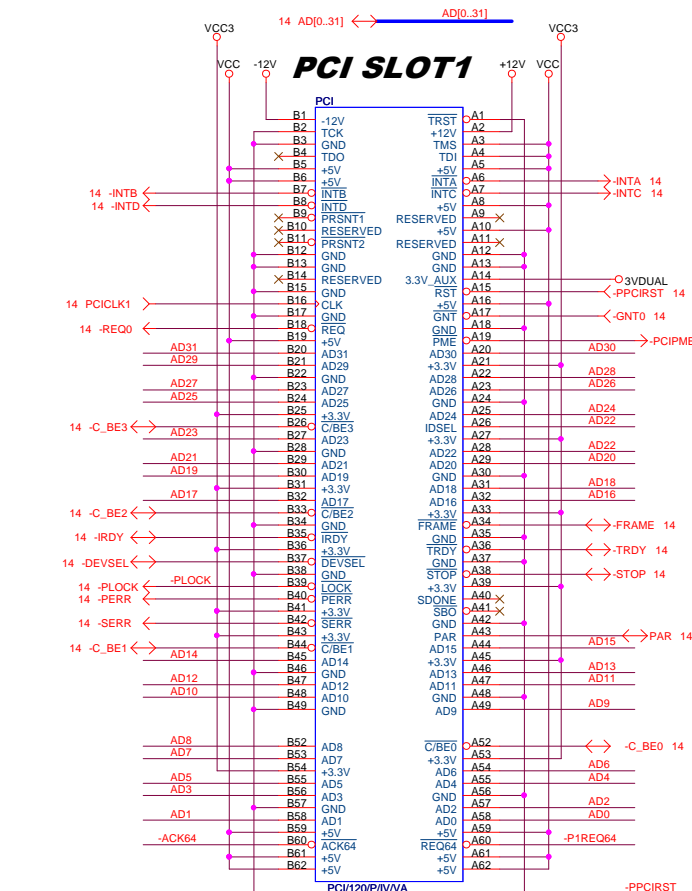
Title			ATI SB950 SATA/IDE/HWM/SPI
Size	Document Number	Rev	1.1
Custom	GA-990FXA-D3		
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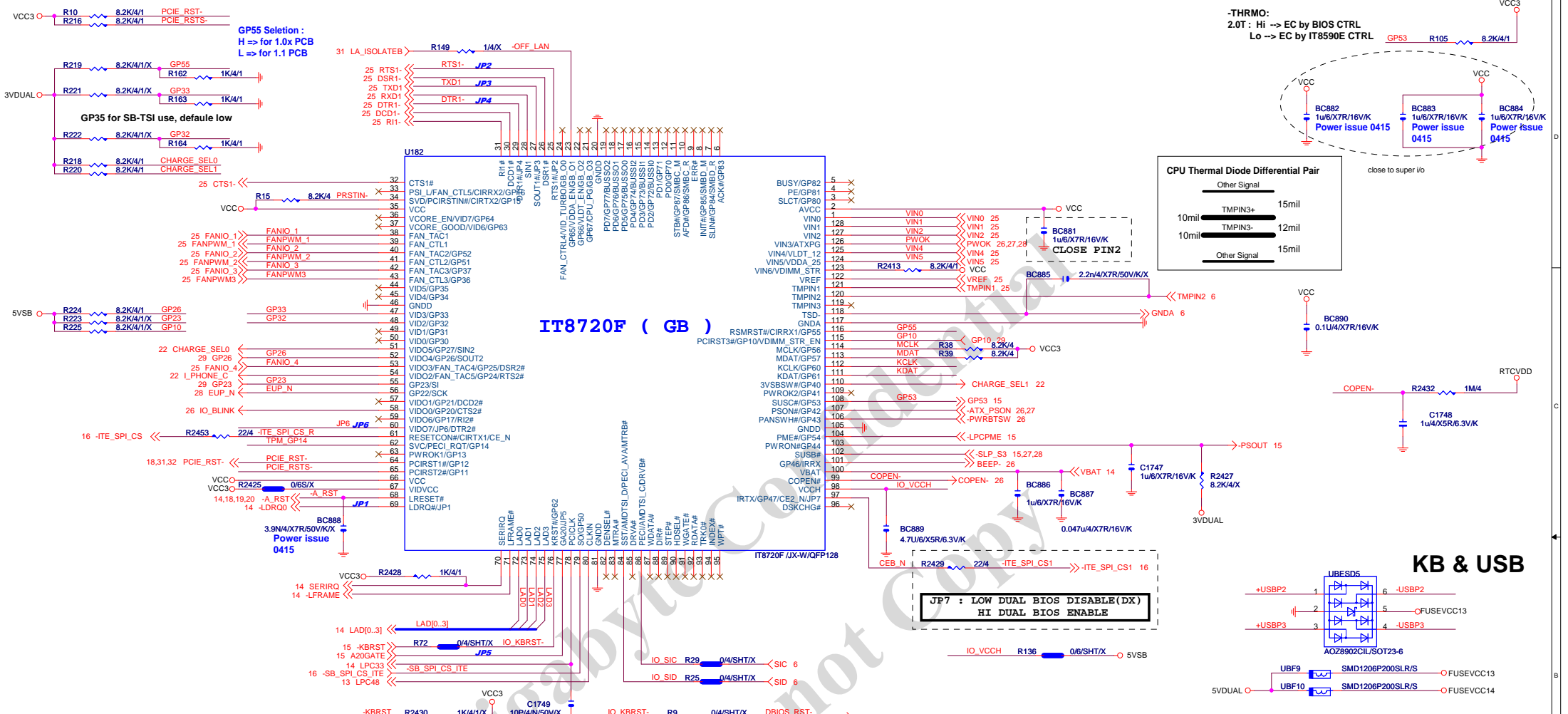


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

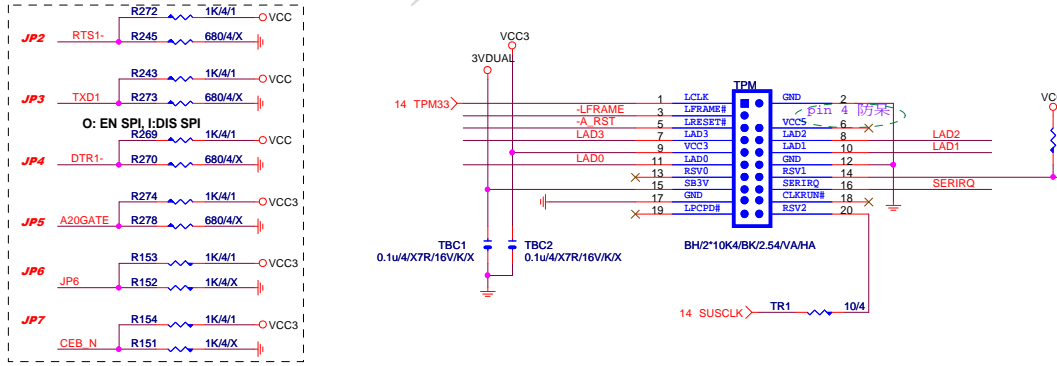


PCI SLOT1





IT8720GB Power On Strapping Options			
Symbol	value	Description	
JP1	Flashseg1_EN	1	Disabled.
Pin 69		0	Flash I/F Address Segment 1 is enabled
JP2	VIDO_EN	1	Disable VID output pins
Pin 25		0	Enable VID output pins
JP3	CHIP_SEL	Chip selection in Configuration	
Pin 27			
JP4	K8PWR_EN	1	K8 power sequence disabled
Pin 29		0	K8 power sequence enabled
JP3 & JP5	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
Pin 27 & Pin 77		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5	WDT_EN	1	Disable WDT to rest PWROK
Pin 77		0	Enable WDT to rest PWROK
JP6	SVID_EN	1	Disable SVID Function
Pin 60		0	Enable SVID Function
JP7	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
Pin 97		0	Disable Dual BIOS Function for GigaByte Only

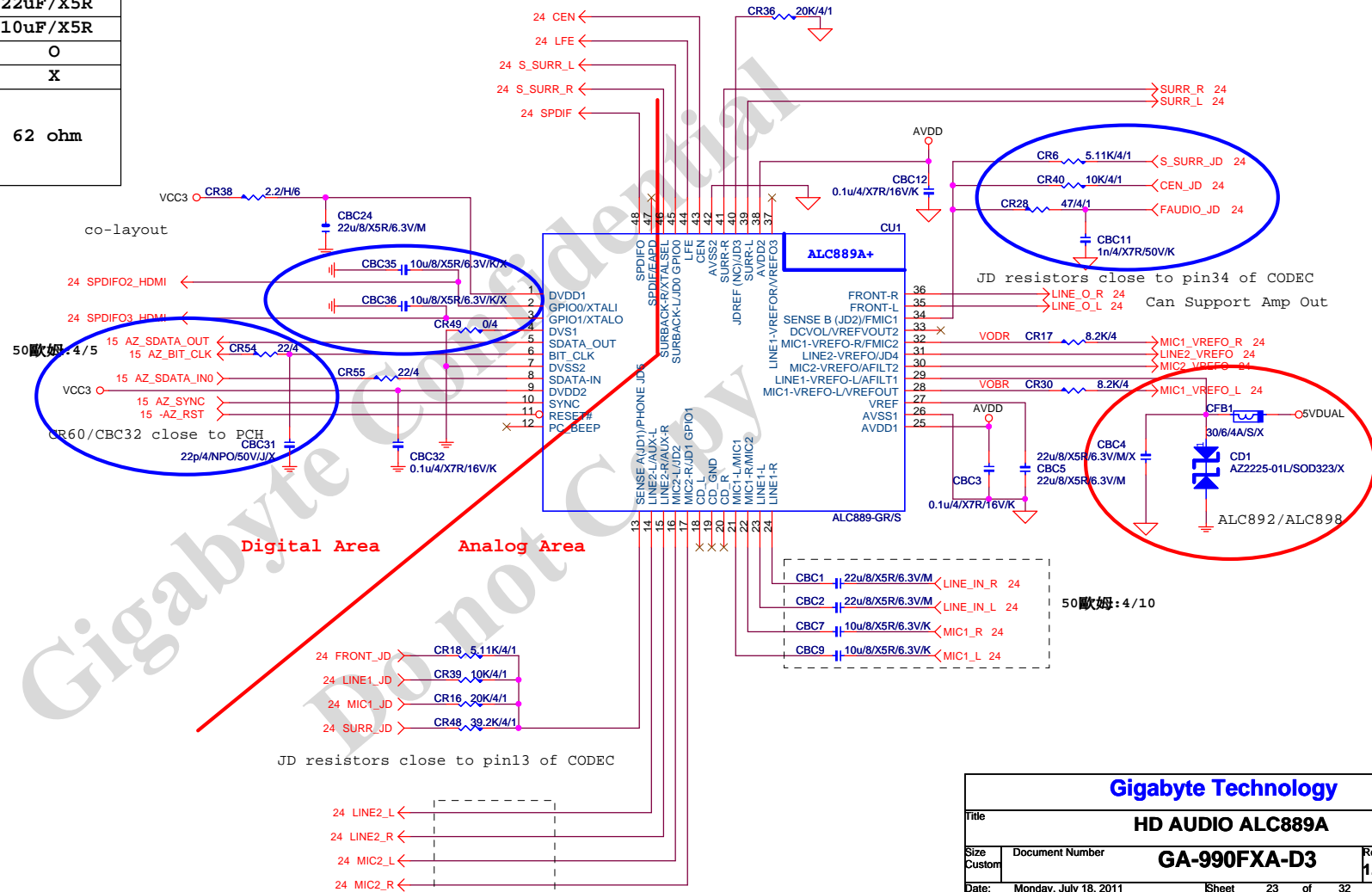


GIGABYTE™

ITE 8718 LPC IO ,Dual-BIOS

Title	Document Number	Rev
Size	Customer	GA-990FXA-D3
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	ALC889	ALC889B	ALC898/ALC892
CR65	O	O	X
CBC35	X	X	10uF/X5R
CBC39	X	10uF/X5R	X
CR31	O	X	O
CR66	X	O	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC5/CBC6/CBC9/CBC11	10uF/X5R	10uF/X5R	10uF/X5R
CR51/CD1/CBC7	X	X	O
CD2/CD3/CQ3/CQ5	O	O	X
CR5/CR8/CR1/CR14/ CR17/CR22/CR45/CR33/ CR47/CR40/CR26/CR37/ CR13/CR11/CR57/CR53	62 ohm	62 ohm	62 ohm



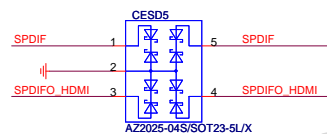
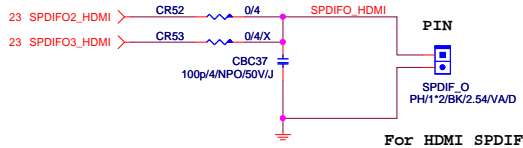
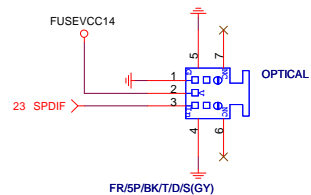
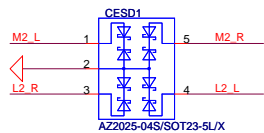
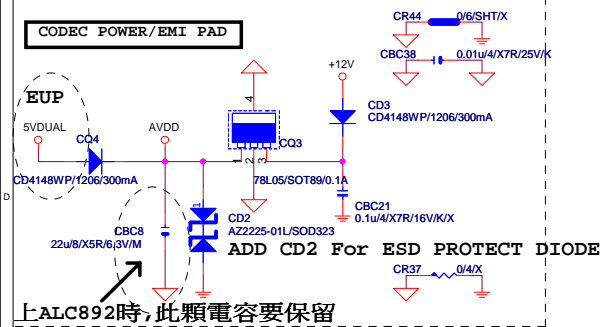
Gigabyte Technology

Title HD AUDIO ALC889A

Size Custom Document Number GA-990FXA-D3 Rev 1.1

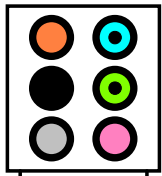
Date: Monday, July 18, 2011 Sheet 23 of 32

CODEC POWER/EMI PAD

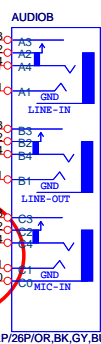
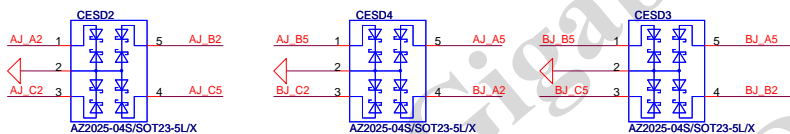


AZALIA JACK

BTX AZALIA CONNECTOR



11NR6-403007-21R



BLUE

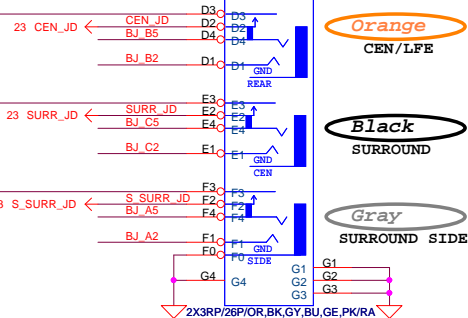
LINE-IN

GREEN

LINE-OUT

PINK

MIC-IN



Orange

CEN/LFE

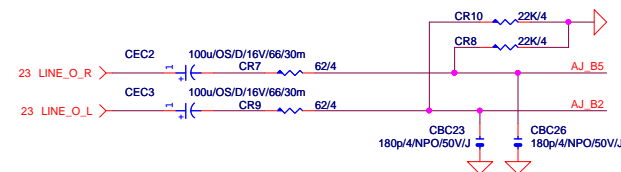
Black

SURROUND

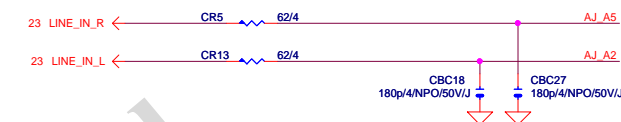
Gray

SURROUND SIDE

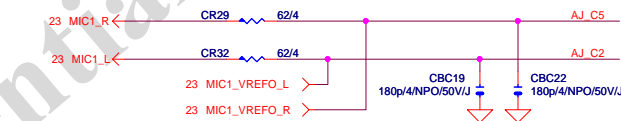
LINE-OUT



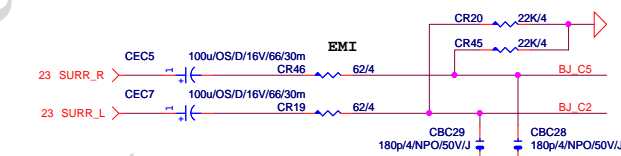
LINE-IN



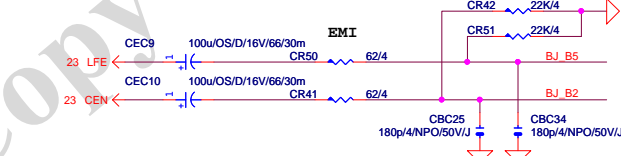
MIC-IN



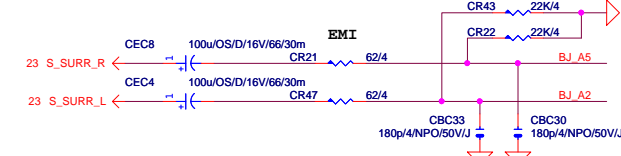
SURROUND



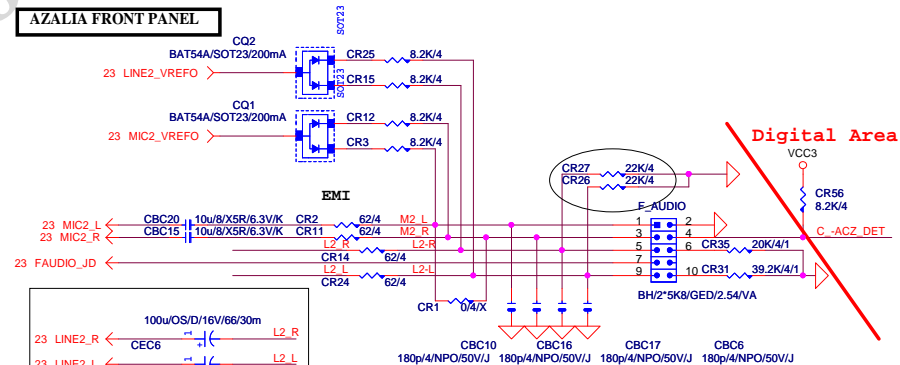
CEN/LFE



SURR BACK

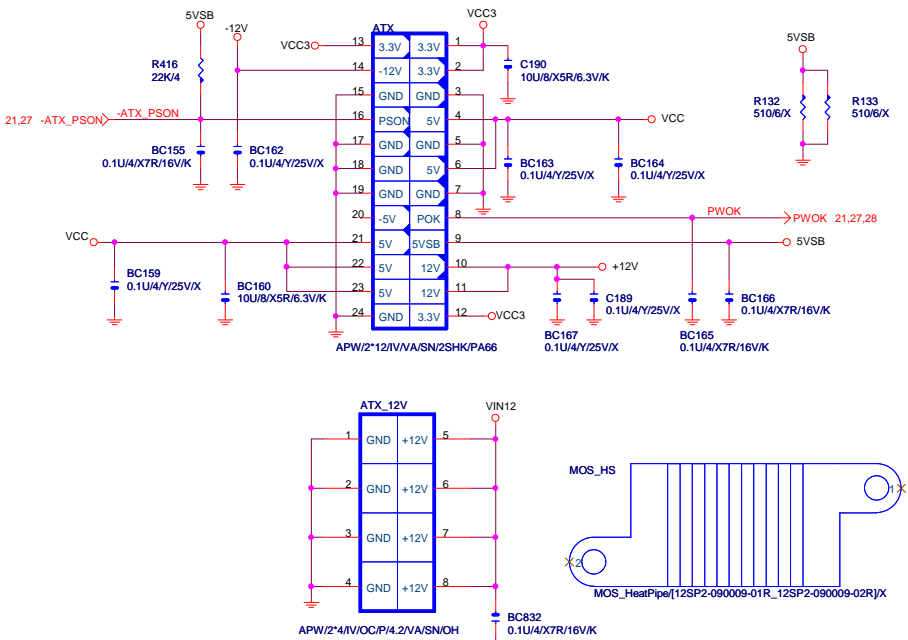
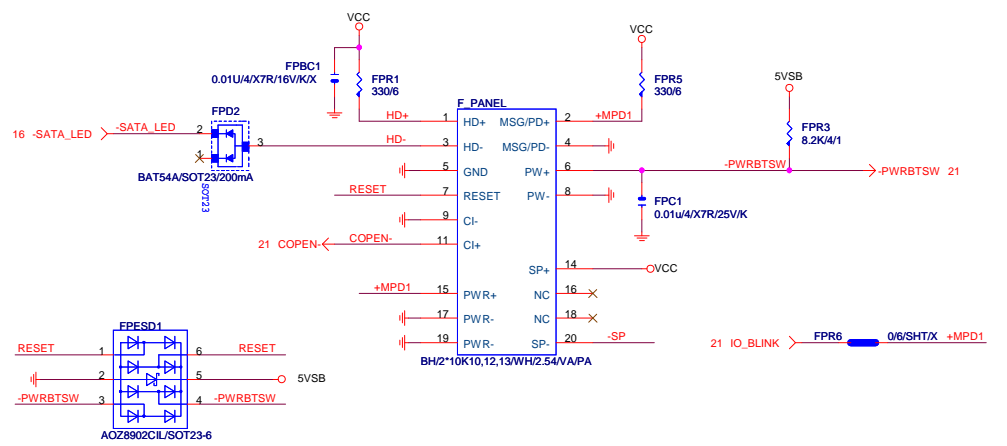
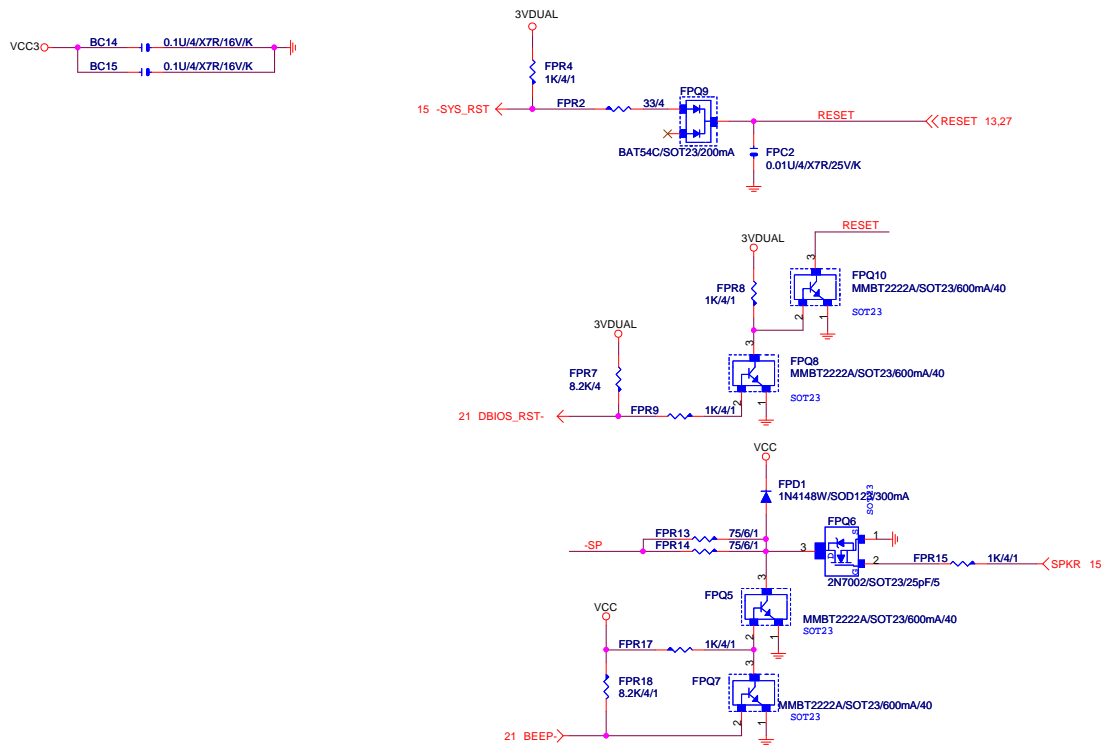


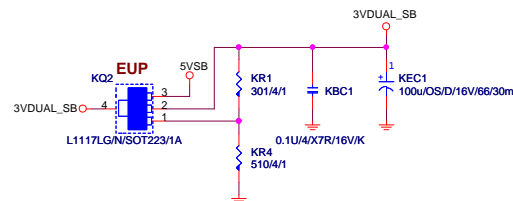
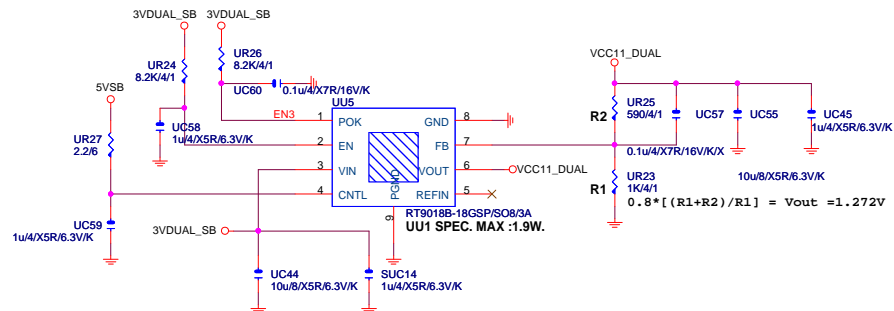
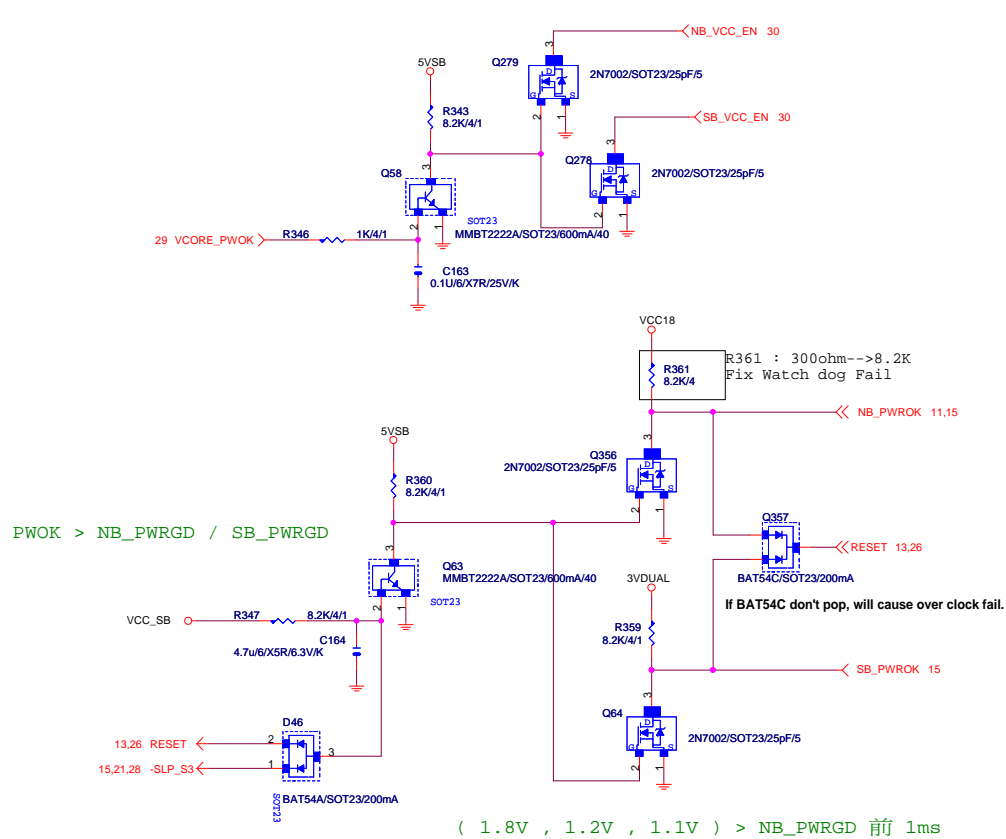
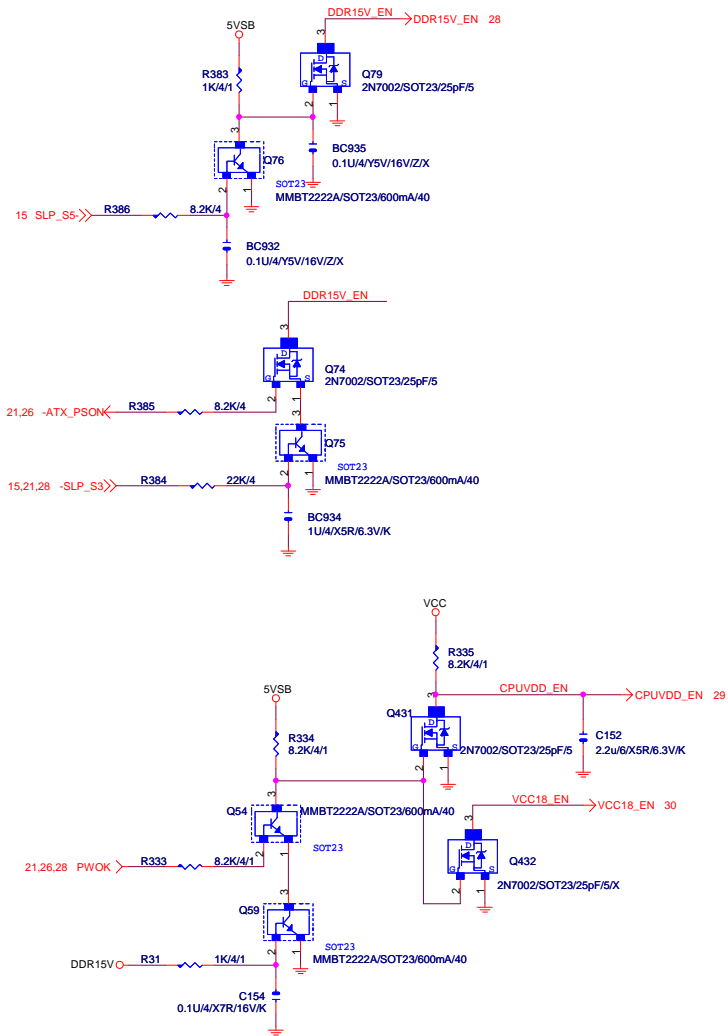
AZALIA FRONT PANEL

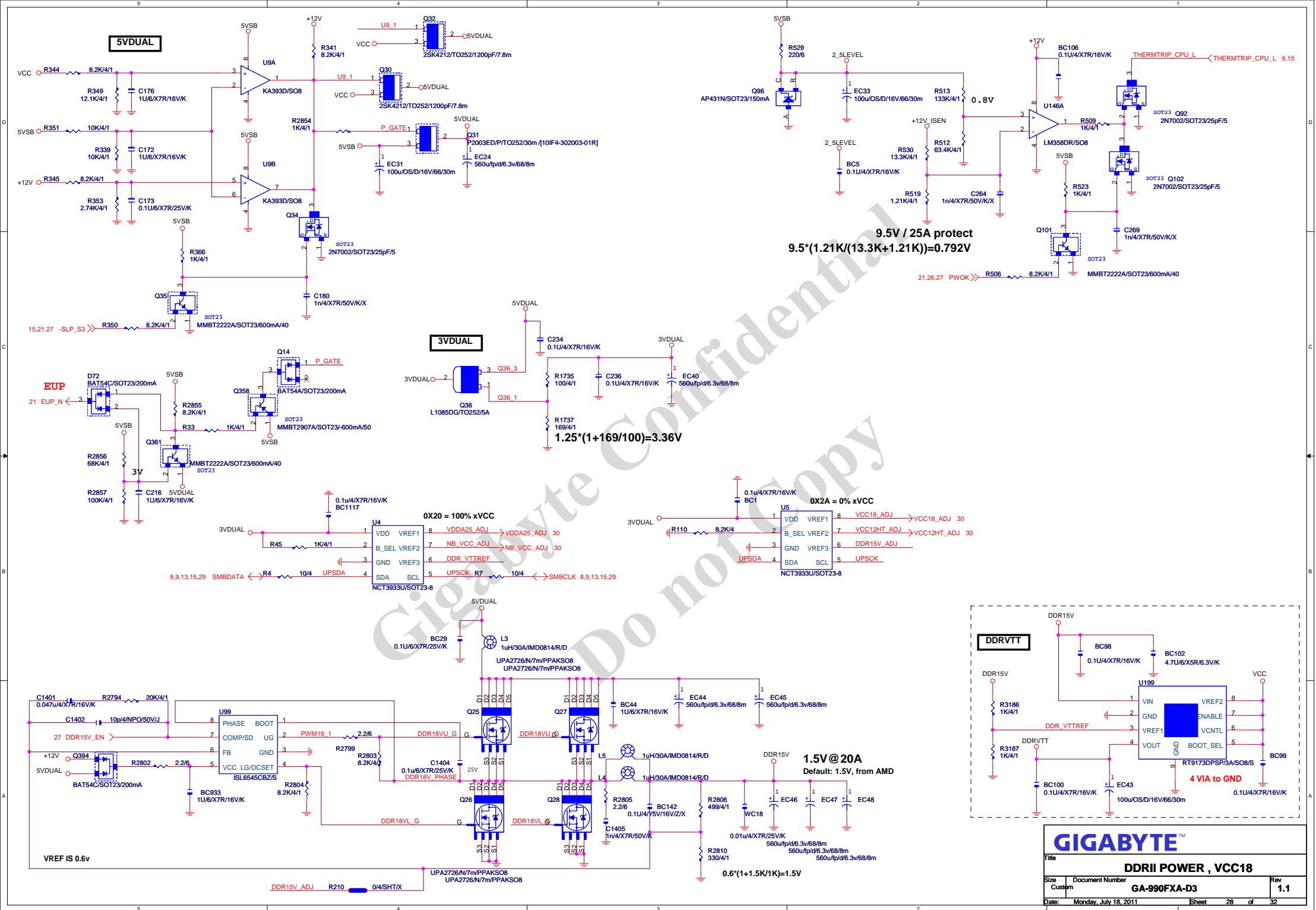


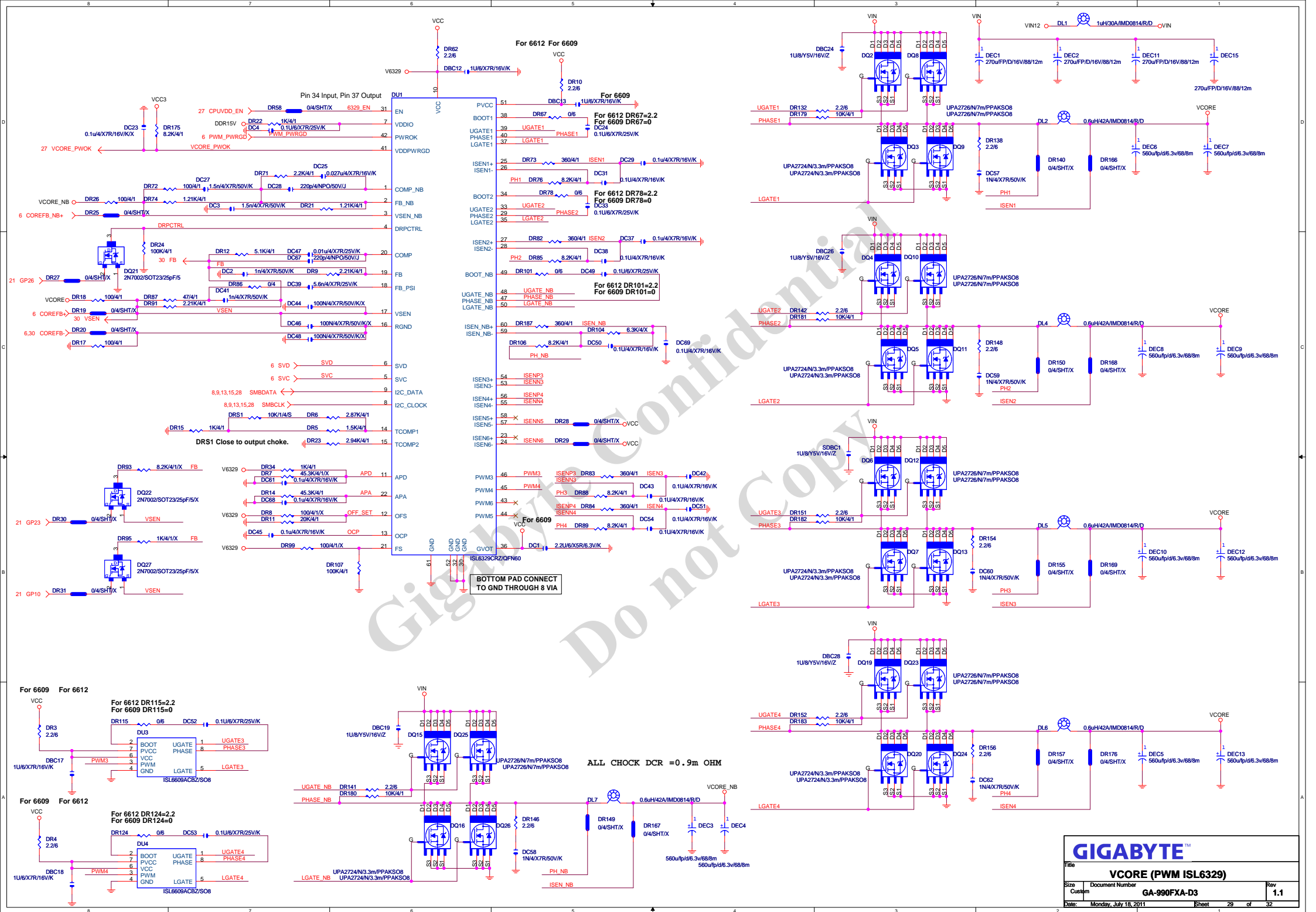
Gigabyte Technology

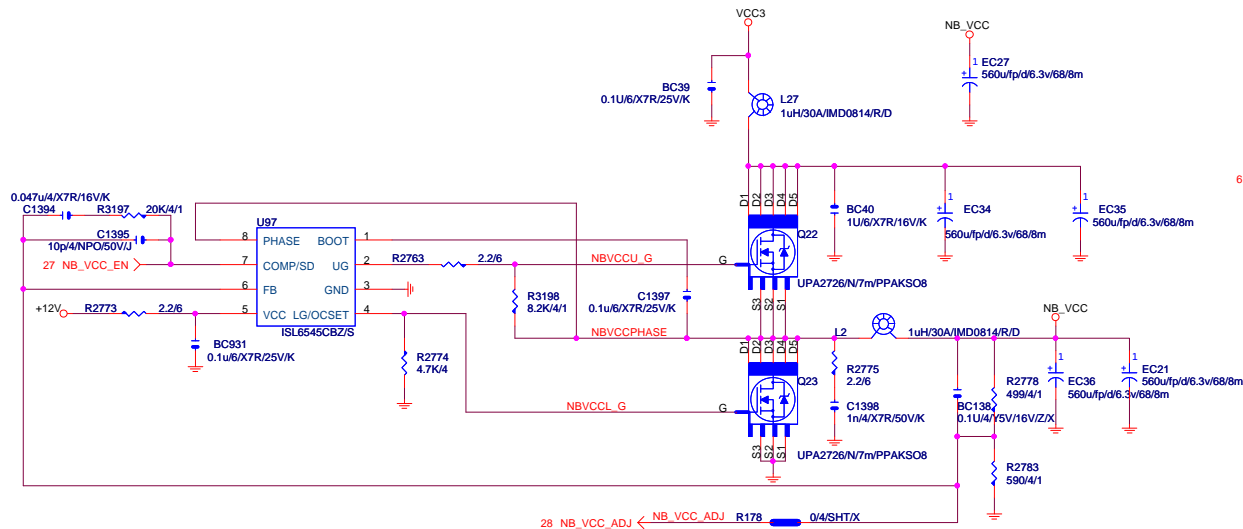
Title		Rev	
AUDIO JACK		1.1	
Document Number		GA-990FXA-D3	
Size	Custom	Monday, July 18, 2011	Sheet 24 of 32





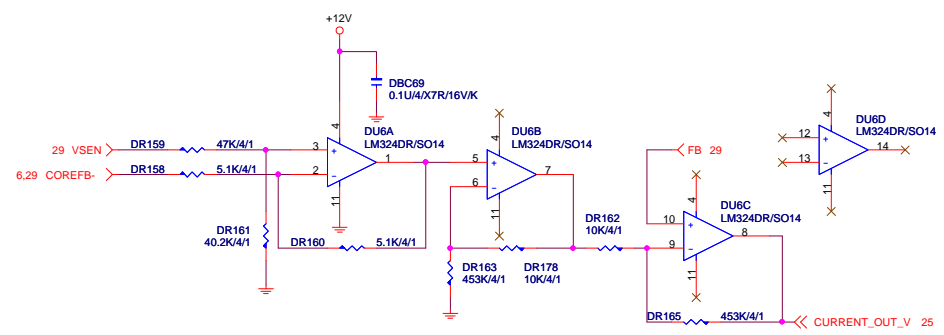
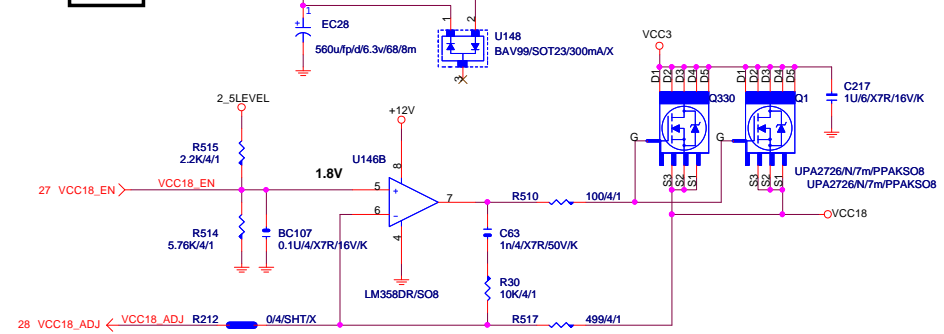




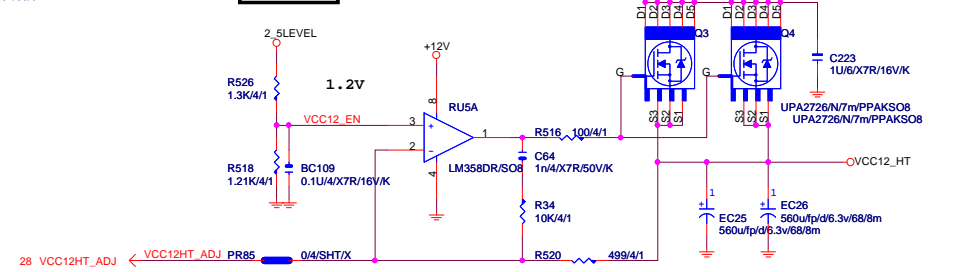


ATI for VCC3/VCC18 power ramp-up 2.1V
U148 for IGP type Only

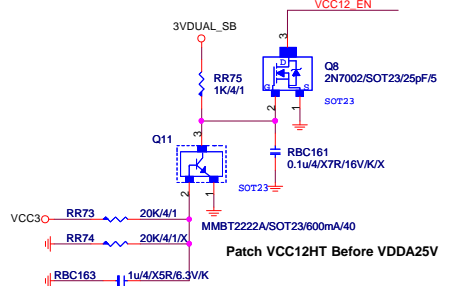
VCC18



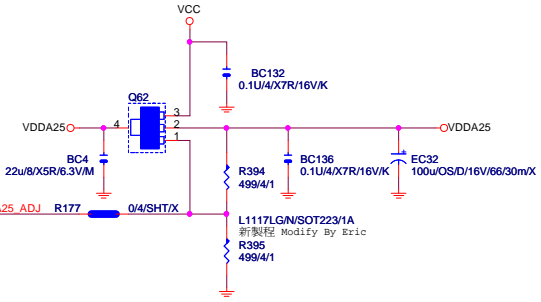
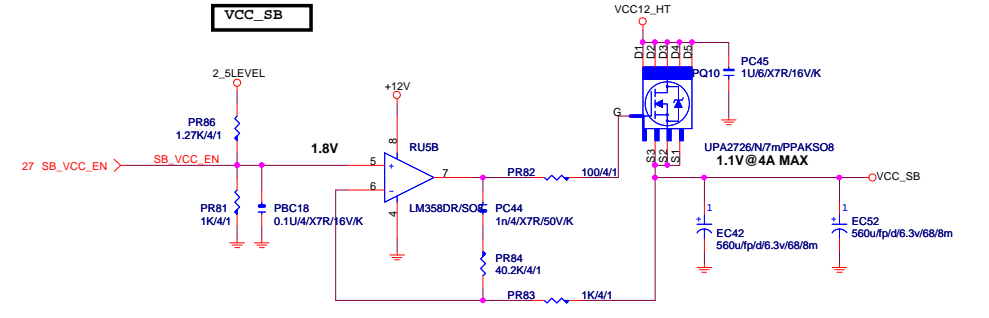
VCC12_HT

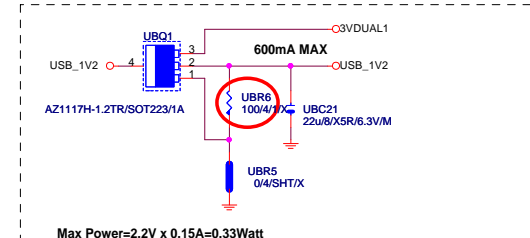
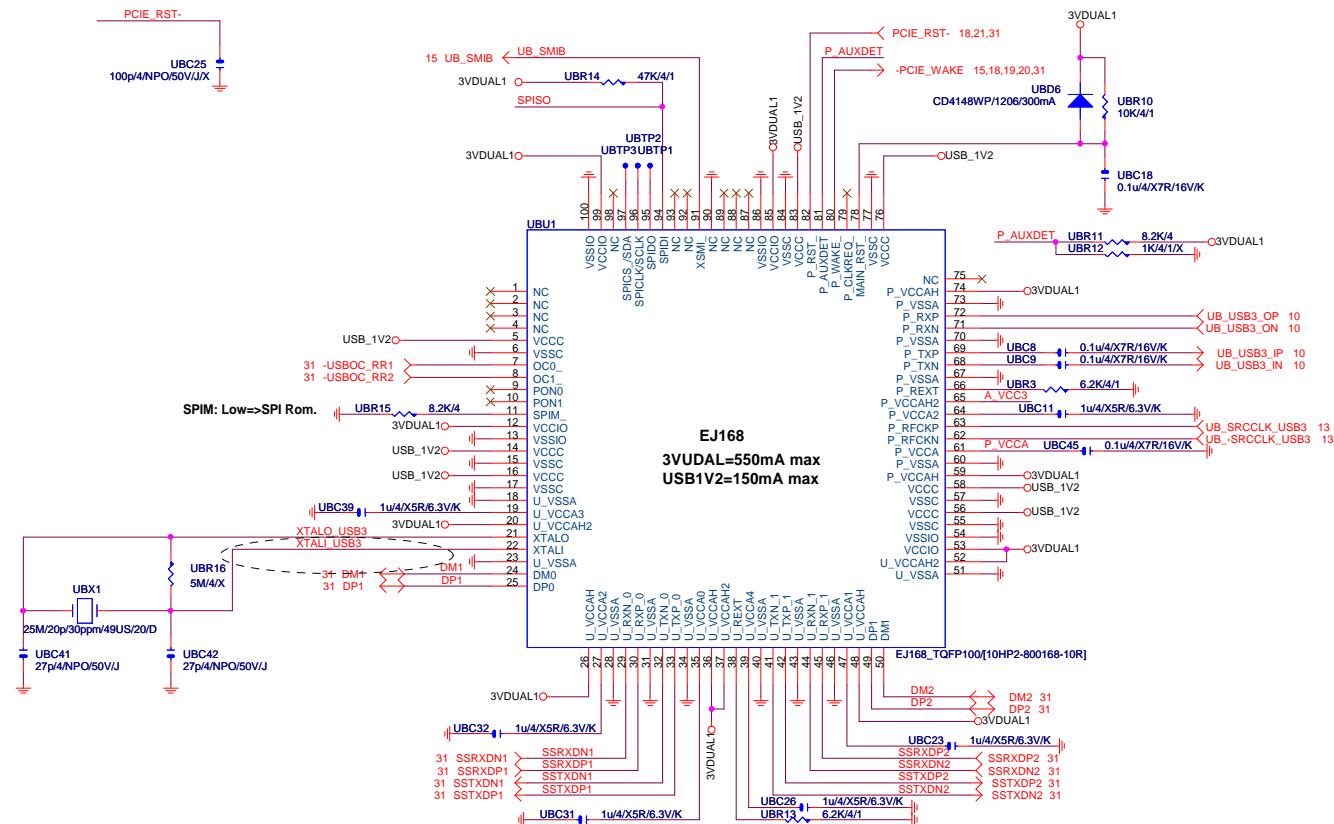
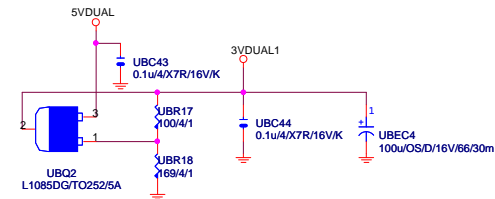
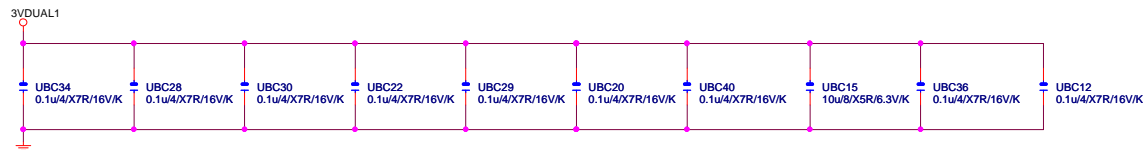


Patch VCC12HT Before VDDA25V

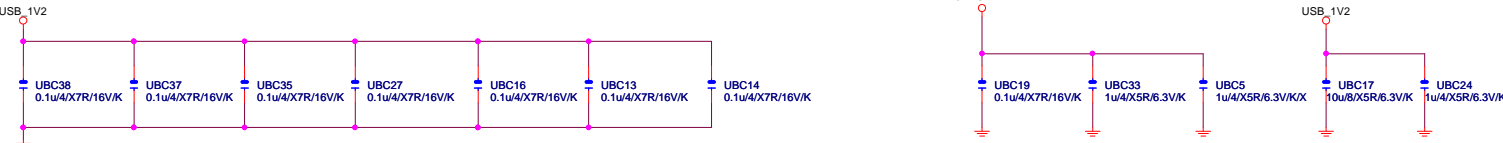


VCC_SB





AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]
L1117LG/N/SOT223/1A-->UR17:0/4,UR16:100/4/1 [1.25V]



USB3.0 --> 5GHz
BANDWIDTH=5GHz*(8b/10b)=4Gb/s=500MB/s

GIGABYTE™			
Title EJ168 R_USB30			
Size Custom	Document Number GA-990FXA-D3	Rev 1.1	
Date: Monday, July 18, 2011	Sheet 32	of 32	